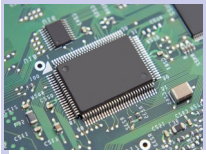

Digital Design Concepts LLC
VHDL Level 1 Online Training Description

Course Description (doc version = 1.0.2)

The VHDL Level 1 Online Training Course is a 16 hour course that is taught with a live instructor. At the conclusion of the course, students will have the ability to design and simulate digital logic circuits using the VHDL language and commercial EDA tools. Approximately 80% of classroom time consists of teacher instruction, while the other 20% of classroom time is dedicated to exercises. At the conclusion of the course, students will be able to perform the following:

- write efficient code using the latest VHDL constructs
- create sophisticated synchronous designs using VHDL primitives, LSI components, and finite state machines
- create hierarchical designs
- write testbenches and simulate designs using Modelsim simulator
- write code that follows good programming style

All students will receive a hard copy of the training materials and exercises several days prior to the start of the class. In addition, several reference designs will be available for download.

Course Topics

- Introduction to RTL languages
- The typical digital design workflow
- VHDL basics
- Data types
  - std_ulogic, std_logic
  - integer, real
  - Enumerated types
  - Constants
  - Vectors
  - Arrays
- Combinational logic design
  - Continuous Assignments
  - Operators
- Procedural logic design
  - Processes
  - Sensitivity list

- Combinational logic using process blocks
- Sequential logic using process blocks
- Flip Flops
- If-else statements
- Case,

- Entities and architectures
- Synthesis
  - Characteristics
  - The FPGA logic cell
  - Synthesis techniques for optimizing designs
- Case studies -- coding for basic LSI modules
  - Flip/Flop register with reset, clock enable
  - Multiplexer implementations
  - Shift registers
  - Counters
  - Comparators
- Hierarchical design
  - Advantages of hierarchical design
  - Instantiation methods
- Generics
- Finite State Machines
  - Mealy, Moore and mixed type machines
  - Two/Three Process formats
  - Encoding/synthesis strategies
- File I/O
- Testbench concepts
  - Procedures
  - Functions
  - Loops
  - Wait
- Functional Simulation
  - Compiling designs
  - Simulating designs
  - Verifying the results
- Good design practices
- Future Topics